#12/Appeal Brief
Hawkins
12/17/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Murphy	Docket No:	TI-33069
Serial No:	09/898,555	Examiner:	Gonzalez, J.
Filed:	07/02/01	Art Unit:	2834
For:	OUTPUT VOLTAGE SENSING OF CHARGE AND VOLTAGE MODE ACTUATOR DRIVES		

APPEAL BRIEF PURSUANT TO 1.192(c)

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on 11-4-02.

Tommie Chambers

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final rejection mailed May 20, 2002, and the Advisory Action mailed August 19, 2002.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellant's legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

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STATUS OF THE CLAIMS

The application was originally filed with Claims 1-23. Claim 4 was cancelled. Thus, the subject matter of the instant application is Claims 1-3 and 5-23.

STATUS OF AMENDMENTS

The Application was originally filed with Claims 1-23.

By virtue of the amendment filed on February 11, 2002, Claim 4 was canceled. Additionally, by virtue of the same amendment, Claims 1-3, 18, and 22 were amended. An amendment after Final Rejection was filed on July 23, 2002 that attempted to amend Claims 5 and 22. However, the Examiner in the advisory action did not enter the proposed amendment.

SUMMARY OF THE INVENTION

Referring now to Figure 2, circuit 40 is seen to include a differential drive amplifier 42 having an inverting input connected to a voltage reference V_{ref}, and a non-inverting input coupled to and controlled by a AC command signal provided by a digital to analog converter (DAC) as will be discussed shortly. Driver 42 is seen to have a 1X output that is placed at a capacitor shown as C_{piezo}.

Circuit 40 is seen to further comprise of a low frequency voltage nulling loop around the charge control driver circuit 42 including an operational amplifier 44.

A feedback capacitor C1 is provided such that amplifier 44 is configured as a high frequency integrator. The feedback path from the OUT6XP output to the input of the driver 42 provided through the integrating DC restore amplifier 44 advantageously has the effect to null any DC offsets at the capacitor C_{piezo}.

This resistor R2 is connected to the DC restore amplifier and allows for a low frequency DC coupled path and thus allows the DC positioning of the piezo in the charge mode to be changed.

Referring now to Figure 3, there is depicted both the AC response and DC response of circuit 40.

Turning now to Figure 4, there is depicted a more detailed schematic of circuit 40, whereby the driver 42 is shown as amplifier 54 with feedback selectable by switches. The DC restore amplifier is depicted as amplifier 52 with its feedback and switches that select between charge and voltage mode. A four-bit digital-to-analog converter (DAC) 50 is seen to provide the DC command input to the inverting input as shown.

Figure 5 depicts the active circuitry when the circuit is operating in the charge mode, and Figure 6 illustrates the active circuitry of circuit 40 when the circuit operates in the voltage mode.

When in the voltage mode, the circuit operates with feedback capacitor C1 provided externally. The offset DAC is not active.

The features include the charge mode operation being provided for varying number of piezo elements, how the operation is maintained when normal offsets from processing are present, and how a DC coupled input is provided in conjunction with the DC restore operation.

The first advantageous feature is how the charge mode solution allows for a varying number of piezo elements. This is accomplished by setting up a voltage mode feedback on the OUT1X output using the amplifier 42.

If the load on OUT6XP, which is the main point of interest since the piezo element will be connected there, changes due to a different number of piezo elements used (this is common place for piezo actuator applications where a different number of actuators are being driven depending on the system configuration), then the output charge gain needs to be changed according to the number of piezo elements on the output.

Advantageously, this is accomplished by correspondingly switching the gain of the feedback on OUT1X and thus change the overall charge gain.

Therefore, the solution for changing the gain on the OUT1X is done with the overall feedback resistance changing using switches G0Z, G1Z and G2Z such that the RC product on the OUT1X is matched to the changing RC on OUT6XP, which changes with the number of piezo elements, – and this is a key feature also provided by the solution.

The advantageous second feature is how the DC restore amplifier 44 is used to compensate for offsets in the OUT1X/OUT6XP circuit chain. There will be some current mismatch when the amplifier chain is manufactured, and this mismatch could cause the OUT6XP output to saturate into one rail or the other. This would make the solution non-usable and make the charge mode solution useless. A feedback path from the OUT6XP output to the input of the amplifier 42 is provided through the integrating DC restore amplifier 44. The effect of the feedback is to null any DC offsets.

The advantageous third feature is the DC coupled input. As mentioned above, the DC restore feature creates an AC coupled solution from DAC input to the OUT6XP output (piezo drive node). It is desired to also have some control, from a DC coupled standpoint, as to where the OUT6XP output tends to at DC. This is accomplished with another input feature added through the offset DAC into a resistor. This resistor R2 is connected to the DC restore amplifier and allows for a low frequency DC coupled path and thus allows the DC positioning of the piezo in charge mode to be changed.

Referring now to Figure 10, there is generally shown at 100 a piezo actuator drive circuit having a piezo actuator adapted to be sensed in the voltage mode or the charge mode, wherein like numerals to those shown in earlier discussed Figures refer to like elements. The sensing mode of the present invention achieves technical advantages by switching the output of the drive amplifier 42 to a high impedance state, and disconnecting the output mirrors.

The output sensed voltage from the piezo actuator is used to determine how much the piezo actuator load has varied, and can be used to compensate for previously mentioned unwanted defects.

To characterize the piezo actuator C_{piezo} in the sensing mode, the charge on the piezo actuator induces a voltage drop across the resistive divide network shown as resistors R_1 and R_2 forming a portion of the feedback in the voltage mode. The output of this resistive divide network, that is, the node between resistors R_1 and R_2, is provided to a sensing amplifier shown at 102 forming a buffer and subsequently feeding a resistive divide network shown as resistors R_3 and R_4. The output is sensed between resistors R_3 and R_4 and provided to the analog-to-digital converter (ADC). This sensed signal is indicative of the piezo actuator i.e. position and allows the circuit to characterize the changes of the load.

Referring to Figure 11, there is depicted the DAC input signal at 104, the output OUT6XP signal at 106, and the command signal used in the sensing mode at 108. As shown, the output signal 106 moves as a function of the feedback resistors R_f, R_i, R_1 and R_2.

Referring to Figure 13, there is depicted the DAC input as signal waveform 202. Output OUT6XP is shown at 204, output OUT1X is shown at 206, the control signal for the sense mode is shown at 208, and the input signal for the ADC, which is the output of the sensing buffer, is shown at 210.

ISSUES

The three issues on appeal are first whether or not Claims 2, 3, 18, 19, and 20 are patentable under 35 U.S.C. §112, second paragraph, second whether Claims 1-3, and 5-19 are unpatentable under 35 U.S.C. §103 over Wilson in view of Fontanella; and thirdly whether Claims 20-23 are unpatentable under 35 U.S.C. §103 over Wilson in view of Konduo.

GROUPING OF THE CLAIMS

Claim 1 as contained it the attached Appendix is independently patentable, and this rejected claim does not stand or fall together for the reasons most clearly set forth herein below.

ARGUMENTS

The Honorable Board's attention is directed to the fact the that Applicants have attempted to amend Claims 5 and 22 but the Examiner has refused to enter these claims.

Claims 2, 3, 18, 19, and 20 were rejected under 35 U.S.C. §112, second paragraph as being indefinite.

These rejections are respectfully traversed in part.

The Examiner questions the charge mode and the voltage mode.

The Honorable Board's attention is directed to page 9, line 9 et seq. where these modes are explained.

With respect to Claim 18, the Honorable Board's attention is directed to Claim 17 where the first output is described.

Claims 1-3 and 5-23 are in full compliance with 35 U.S.C. §112.

Turning now to the art rejections, Claims 1-3 and 5-19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wilson in view of Fontanella; and Claims 20-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wilson in view of Kondou.

These rejections are respectfully traversed.

It is respectfully submitted that Wilson does not disclose or suggest the presently claimed invention including a piezo actuator drive circuit to drive a disk.

Wilson is directed to an ultrasonic generator and consequently could not disclose or suggest the presently claimed invention.

It is respectfully submitted that Fontanella does not disclose or suggest the presently claimed invention including a drive amplifier adapted to drive a piezo actuator in a voltage mode and in a charge mode.

Fontanella discloses a driver circuit for controlling a piezo actuator only the in charge mode. However, nothing in Fontanella discloses a drive amplfiier to drive a piezo actuator in both and voltage mode and a charge mode.

Whether or not Kondou discloses a DC control circuit, a compensation loop, a DAC, and an ADC and whether one of ordinary skill in the art would consider modifying Wilson is of no moment since the result in construction would in no way disclose or suggest the presently claimed invention.

None of the references either separately or in combination could achieve the advantage described.

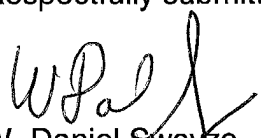
It is respectfully submitted that Claims 1-3, and 5-23 patentably define over the applied art.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-3 and 5-23 under 35 U.S.C. § 112 and 103 are not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



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APPENDIX

1. A piezo actuator drive circuit to drive a disk, comprising:

a drive amplifier having an input, and an output adapted to drive a piezo actuator in a voltage mode and a charge mode; and

a sensing circuit coupled to the drive amplifier sensing a parameter of the piezo actuator.

2. The drive circuit as specified in Claim 1 wherein the sensing circuit is selectively coupled to the piezo actuator in said voltage mode.

3. The drive circuit as specified in Claim 1 wherein the sensing circuit selectively coupled to the piezo actuator in said charge mode.

5. The drive circuit as specified in Claim 1 wherein the sensing circuit provides a signal indicative of the piezo actuator position.

6. The drive circuit as specified in Claim 1 wherein the sensing circuit comprises a resistor divider providing a voltage signal.

7. The drive circuit as specified in Claim 6 wherein the voltage signal varies proportionally to the piezo actuator load.

8. The drive circuit as specified in Claim 1 wherein the drive amplifier has a feedback, wherein the sensing circuit is a portion of the feedback.

9. The drive circuit as specified in Claim 5 wherein the signal is indicative of the piezo actuator load variation.

10. The drive circuit as specified in Claim 1 further comprising a current mirror selectively coupled to the output of the drive amplifier.

11. The drive circuit as specified in Claim 10 wherein the current mirror is selectively uncoupled from the drive amplifier in the sensing mode.

12 The drive circuit as specified in Claim 11 wherein the current mirror is a class AB amplifier.

13. The drive circuit as specified in Claim 1 wherein the drive amplifier has a charge mode feedback configured to allow multiple piezo actuators to be driven in the charge mode.

14. The drive circuit as specified in Claim 13 wherein the charge mode feedback includes a DC restore amplifier forming a portion of the sensing circuitry.

15. The drive circuit as specified in Claim 14 wherein the DC restore amplifier is reconfigured in the sensing mode.

16. The drive circuit as specified in Claim 15 wherein the reconfigured DC restore amplifier is connected in a closed feedback loop in the charge mode, and in an open feedback loop in the sensing mode.

17. The drive circuit as specified in Claim 1 wherein the drive amplifier has a first output, and a second output having a current mirror based on the first output.

18. The drive circuit as specified in Claim 17 wherein the drive circuit includes a capacitor being coupled to the first output and the piezo actuators are adapted to be driven by the second output.

19. The drive circuit as specified in Claim 18 wherein a first time constant formed by the capacitor and the voltage mode feedback, and a second time constant formed by the piezo actuators and the voltage mode feedback, are substantially equal.

20. The drive circuit as specified in Claim 13 further comprising a DC control circuit controlling the DC value at the piezo actuator.

21. The drive circuit as specified in Claim 1 wherein the DC control circuit is integrated into the low frequency compensation loop.

22. The drive circuit as specified in Claim 1 further comprising a digital-to-analog (DAC) coupled to an input of said drive amplifier and a voltage reference being coupled to another input of said drive amplifier.

23. The drive circuit as specified in Claim 1 further comprising an ADC coupled to the sensing circuit.